

FIG. 1 (PRIOR ART)

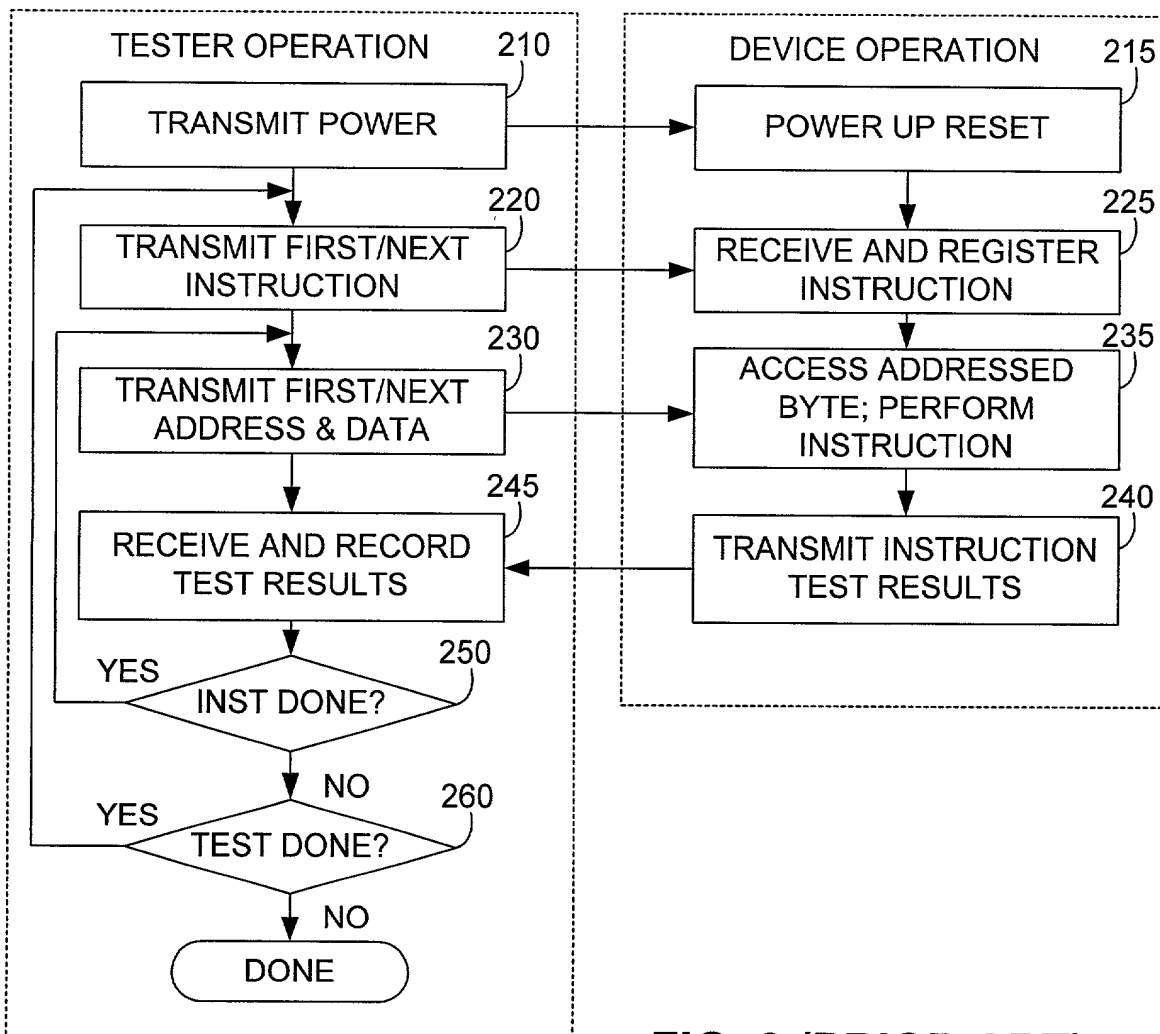


FIG. 2 (PRIOR ART)

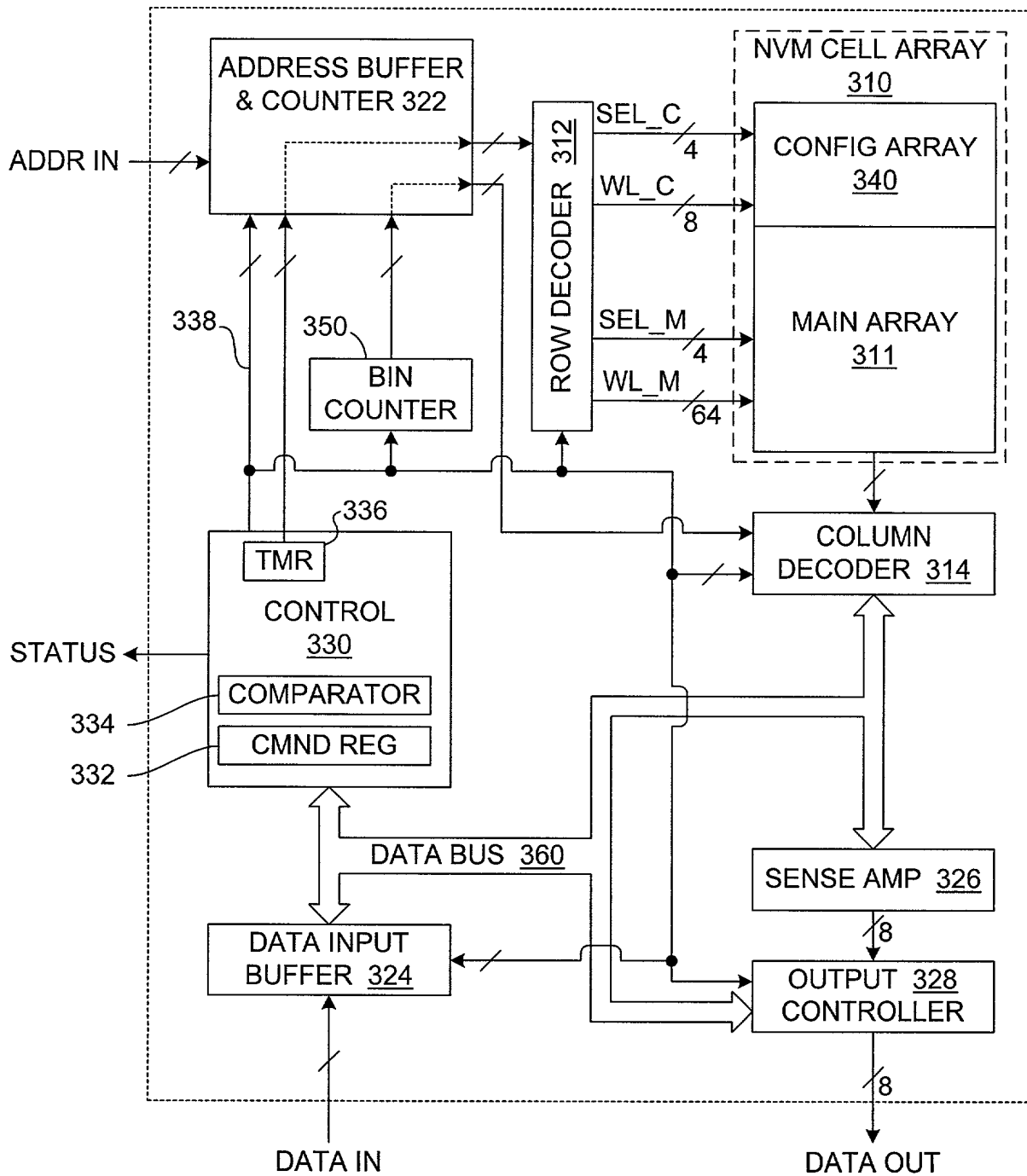


FIG. 3

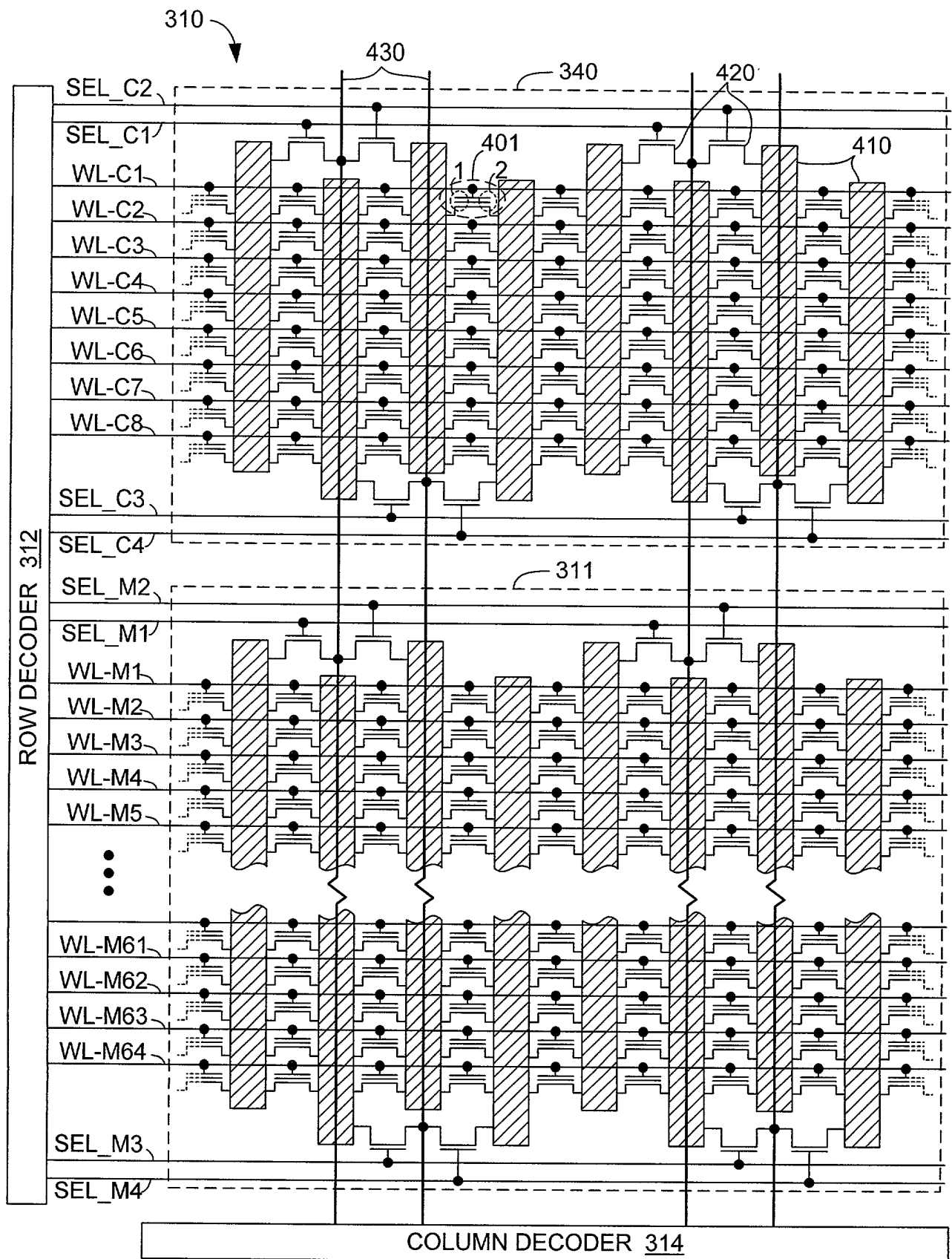


FIG. 4

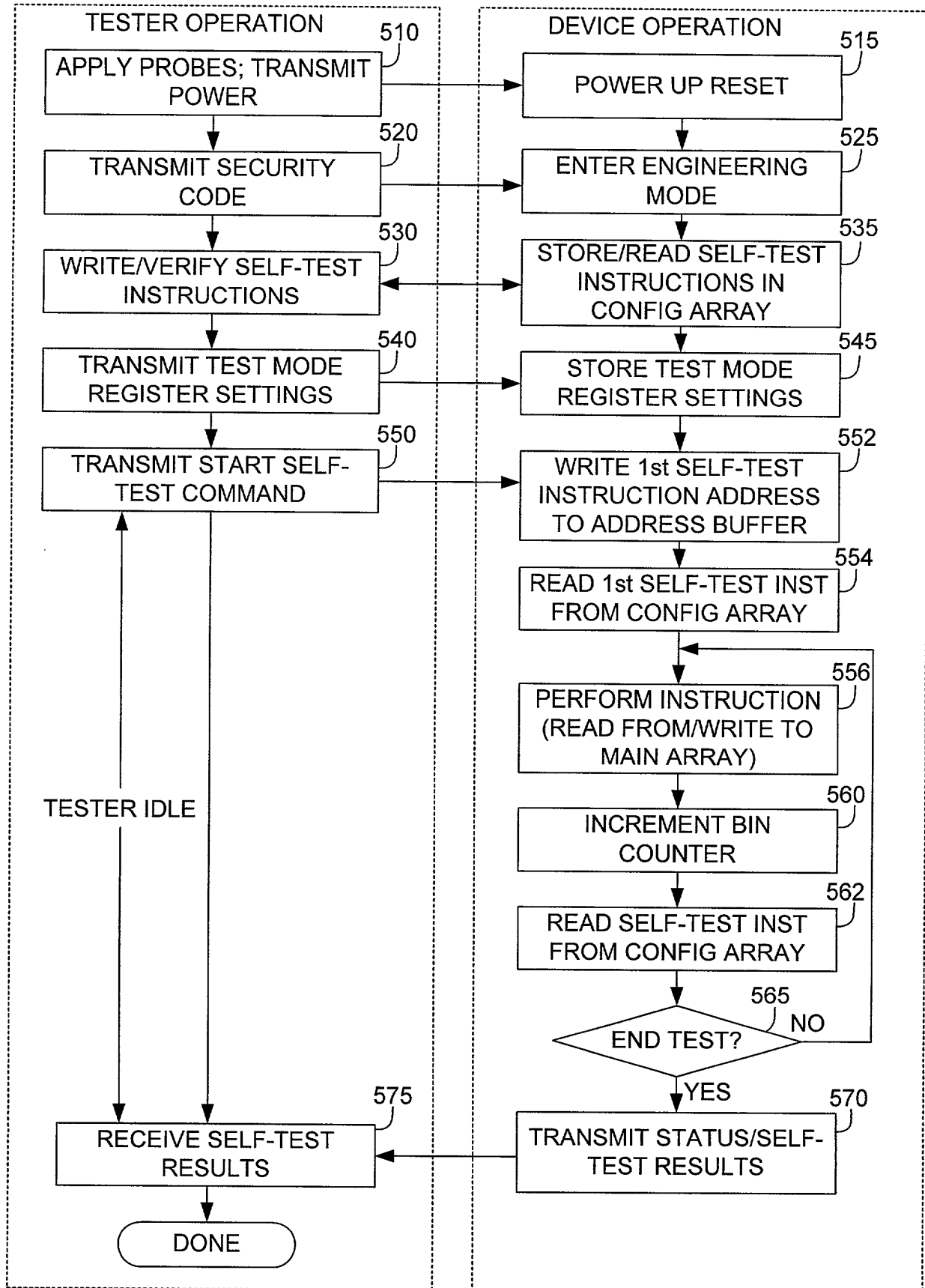


FIG. 5

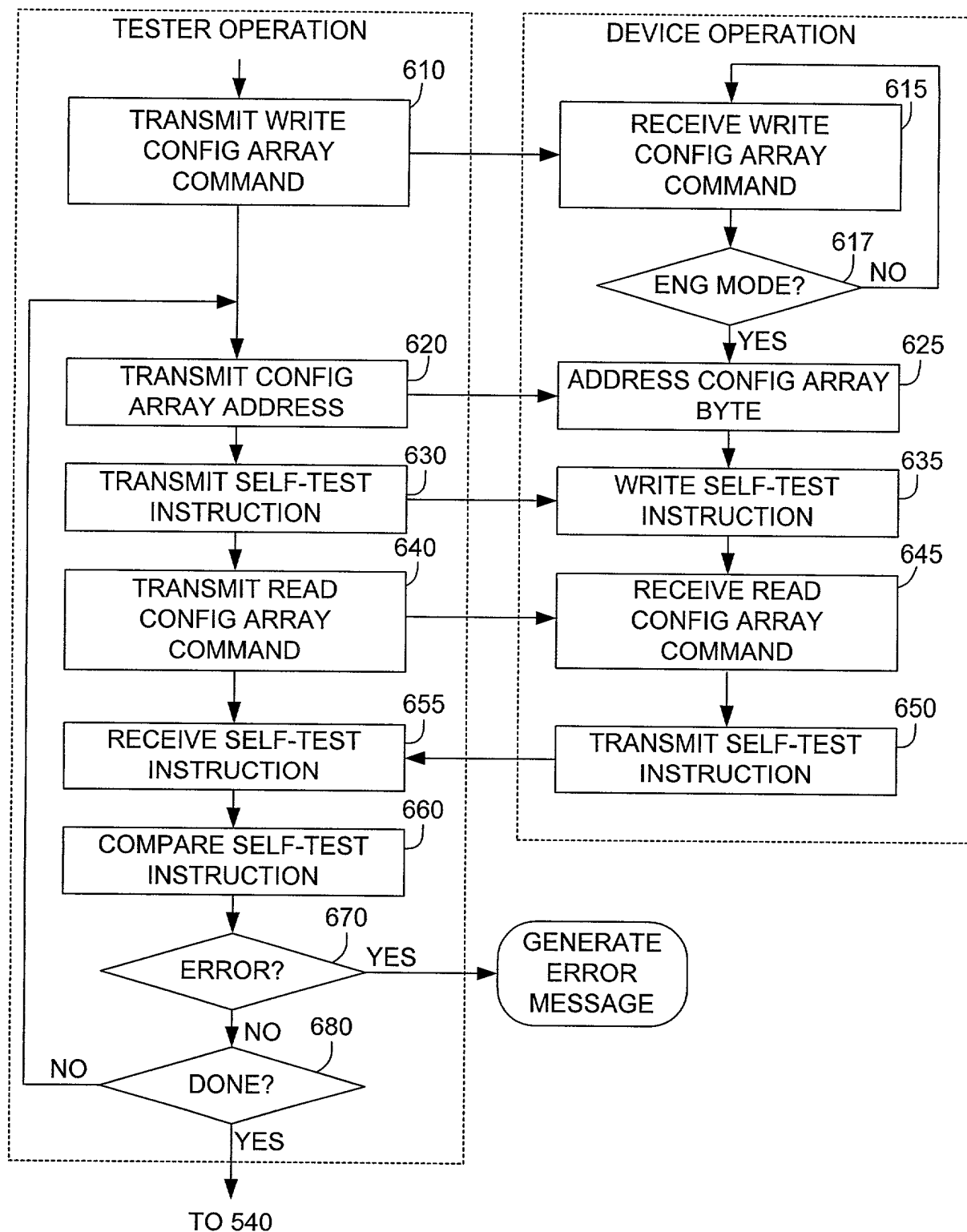


FIG. 6

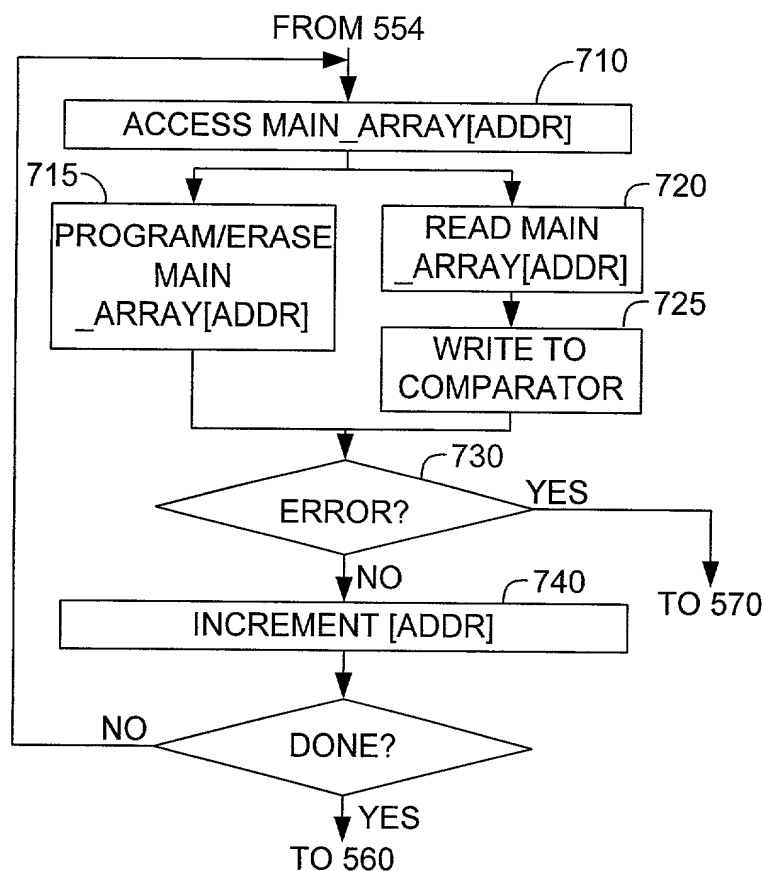


FIG. 7

BIT ADDR	0	0	1	1	2	2	3	3
BYTE 0/1	1	1	1	1	1	1	1	1
BYTE 2/3	1	1	1	1	1	1	1	1
BYTE 4/5	1	1	1	1	1	1	1	1
BYTE 6/7	1	1	1	1	1	1	1	1

FIG. 9(A)

BIT ADDR	0	0	1	1	2	2	3	3
BYTE 0/1	0	0	0	0	0	0	0	0
BYTE 2/3	0	0	0	0	0	0	0	0
BYTE 4/5	0	0	0	0	0	0	0	0
BYTE 6/7	0	0	0	0	0	0	0	0

FIG. 9(C)

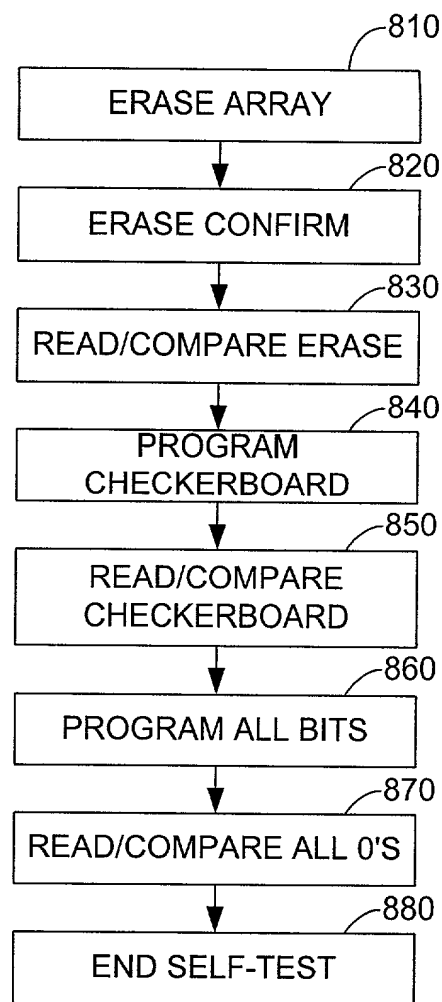


FIG. 8

BYTE 0								
BYTE 1								
BIT ADDR	0	0	1	1	2	2	3	3
BYTE 0/1	0	1	0	1	0	1	0	1
BYTE 2/3	0	1	0	1	0	1	0	1
BYTE 4/5	0	1	0	1	0	1	0	1
BYTE 6/7	0	1	0	1	0	1	0	1

FIG. 9(B)